Vtu Logic Design Laboratory Manual

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VLSI Design Lab Manual Page 2 SYLLABUS VLSI Design Lab (EE-330-F) F - Scheme (w.e.f. August 2009) L T P Sessional : 25 Marks - - 2 Practical : 25 Marks Total : 50 Marks Duration of Exam : 3 hrs. 1) Design of Half-Adder, Full Adder, Half Subtractor, Full Subtractor 2) Design a parity generator

LABORATORY MANUAL

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Laboratory Experiments: 1. Verify (a) Demorgan‟s Theorem for 2 variables. (b) The sum-of product and product-of-sum expressions using universal gates. 2. Design and implement (a) Full Adder using basic logic gates. (b) Full subtractor using basic logic gates. 3. Design and implement 4-bit Parallel Adder/ subtractor using IC 7483. 4.

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DIGITAL ELECTRONICS LAB DO’S DON’ TS 1. Be regular to the lab. 2. Follow proper Dress Code. 3. Maintain Silence. 4. Know the theory behind the experiment before coming to the lab. 5. Identify the different leads or terminals or pins of the IC before making connection. 6. Know the Biasing Voltage required for different families of IC’s and ...

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5. Design an XML document to store information about a student in an engineering college affiliated to VTU. The information must include USN, Name, and Name of the College, Branch, Year of Joining, and email id. Make up sample data for 3 students. Create a CSS style sheet and use it to display the document. 6.

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4. Design and implement the counters. 5. Design and implement the sequential circuits such as registers and sequence generator. Lab experiments list: 1. Simplify the given Boolean expression and to realize them using logic gates/universal gates. 2. Design and implementation of half/full adder and subtracter using logic gates/universal gates. 3.

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